Course Title	Digital Systems II & Laboratory				
Course Code	ECE300				
Course Type	Compulsory				
Level	Bachelor (1st Cycle)				
Year / Semester	3rd Year / 5th Semester				
Teacher's Name	TBA				
ECTS	12	Lectures / week	3 hours / 14 weeks	Laboratories / week	3 hours / 14 weeks
Course Purpose and Objectives	This course builds on the fundamental knowledge acquired during the prerequisite Digital Systems course and teaches the concepts and principles related to advanced digital design. It focuses on the use of Hardware Description Languages and the implementation of digital systems using reconfigurable logic devices. During the laboratory part of the course, students gain hands-on experience on the digital systems design lifecycle using appropriate CAD tools.				
Learning Outcomes	Upon successful completion of this course, students should be able to: • Describe the synchronous design methodology which partitions a system into a control unit section and a data-path section • Develop models of combinational and sequential digital logic circuits using a Hardware Description Language (HDL) • Describe the basic types of reconfigurable logic devices such as simple and complex Programmable Logic Devices (PLDs), and Field Programmable Gate Arrays (FPGAs) • Utilize effectively Computer-Aided Design (CAD) tools for the design of digital logic circuits • Model, simulate, verify, and test digital systems using reconfigurable logic devices such as simple and complex Programmable Logic Devices (PLDs), and / or Field Programmable Gate Arrays (FPGAs) • Describe the concept of a Finite State Machine (FSM), and utilize effectively appropriate FSM modelling tools such as state and timing diagrams				
Prerequisites	ECE200	Co-requisites	None		
Course Content	**Theoretical part** Basic concepts: Review of fundamental digital logic concepts, Boolean algebra, design of combinational circuits and function minimization tools, design of circuits with memory, flip-flops, sequential circuits, Finite State Machines, Mealy and Moore FSMs,				

	state-reduction, synchronous design using control section and data-path section. Introduction to HDL (VHDL, Verilog, or SystemC): Computer-Aided Design of digital systems, history and types of HDLs, modelling of fundamental logic elements using HDLs, structural and behavioural modelling using HDLs, design flow, compilation, simulation, and synthesis of HDL code, case studies. Programmable Logic Devices (PLDs): Definition and use of electronic devices which are used to for the development of reconfigurable digital logic circuits, basic types of PLDs, simple PLDs, Read-Only Memory (ROM), Programmable Array Logic (PAL), Programmable Logic Array (PLA), Generic Array Logic (GAL), complex PLDs (CPLDs), Field Programmable Gate Arrays (FPGAs). Algorithmic State Machine (ASM) Charts: Definition and components of ASM Charts, ASM blocks, derivation and realizations of ASM Charts, microprogramming techniques for ASM Charts. Designing Digital Systems with FPGAs: Designing functions and chains on FPGAs, logic blocks, dedicated FPGA features, HDL synthesis, design mapping, placement, and routing for specific implementation technologies. Verification & Testing: Definition and significance of verification in digital systems design, the verification flow, functional verification, timing verification, static timing analysis, design for testability, fault models, testing procedures for combinational and sequential logic circuits, boundary scan and the JTAG standard, memory testing, built-in testing. **Laboratory part** The laboratory part of the course comprises of a set of experiments which complement the theoretical material covered in class. The experiments focus on the implementation of HDL programming (VHDL, Verilog, or SystemC) within an FPGA / PLD Computer-Aided Design environment, for the purpose of designing, simulating, synthesizing, implementing and testing the operation of combinational and sequential logic circuits. FPGA boards will be used as the target of the synthesis process.
Teaching Methodology	Face- to- face
Bibliography	“*Digital Systems Design Using VHDL*” by by Charles H. Roth Jr., and Lizy K. John “*Digital System Design with FPGA*”, by Cem Unsalan, and Bora Tar “*Digital Design: Principles and Practices*”, by John F. Wakerly

<table>
<tr><td></td><td>“Digital Design: With an Introduction to the Verilog HDL, VHDL, and SystemVerilog” by M. Morris R. Mano, and Michael D. Ciletti
“Fundamentals of Digital Logic with VHDL Design”, by Stephen Brown and Zvonko Vranesic</td></tr>
<tr><td>Assessment</td><td><table>
<tr><td>Examinations</td><td>55%</td></tr>
<tr><td>Assignments/Lab</td><td>35%</td></tr>
<tr><td>Class Participation and Attendance</td><td>10%</td></tr>
<tr><td></td><td>100%</td></tr>
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<tr><td>Language</td><td>English</td></tr>
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